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ULTRA LOW-POWER TEST GENERATION BY MERGING OF FUCNTIONAL BROADSIDE TEST CUBES-A SURVEY

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Abstract

To achieve the test compaction with the use of test cube merging. The merging of test cubes is done on the basis of functional broadside test.It is a unique feature of this procedure. It detects all or almost all the transition faults that are detectable by arbitrary (functional and non-functional) broadside test in benchmark circuits.It ensures that the low-power tests would create functional operation conditions in sub circuits that are defined by the test cubes. The parameters area, power, and delay are concentrated to achieve the accurate analysis. Using compression basedschemes test compaction and low power is achieved.

Keywords: Functional broadside tests, low-power test generation, test cubes, transition faults.

I. INTRODUCTION

Testing is to tell whether a system is good or bad. It is used to analyze the fault in transistors, chip etc.Fault is a major concern,it may occur at any time of design, process, package and field. There are two major fields in testing,

ATPG (Automatic Test Pattern Generation):

- Fault simulation
- Test generation

Testable design:

- Design for testability
- BIST
- Synthesis for testability

ATPG (acronym for both **A**utomatic **T**est **P**attern **G**eneration and **A**utomatic **T**est **P**attern **G**enerator) is an electronic design automation method/technology used to find an input (or test) sequence that, when applied to a digital circuit, enables automatic test equipment to distinguish between the correct circuit behavior and the faulty circuit behavior caused by defects. The generated patterns are used to test semiconductor devices after manufacture, and in some cases to assist with determining the cause of failure. The effectiveness of ATPG is measured by the amount of modeled defects, or fault models, that are detected and the number of generated patterns. These metrics generally indicate test quality (higher with more fault detection's) and test application time (higher with more patterns). ATPG efficiency is another important consideration. It is influenced by the fault model under consideration, the type of circuit under test (full scan, synchronous sequential, or asynchronous sequential), the level of abstraction used to represent the circuit under test (gate, register-transfer, switch), and the required test quality.A scan-based test may dissipate significantly more power than possible during functional operation. This led to the development of design-for-testability approaches and test generation procedures that reduce the power dissipation of scan-based tests.Scan based tests are scan-in and scan-out operation. These procedures address the power dissipation during scan shifting and during functional capture cycles.

Most of the procedures consider the total power dissipation in the circuit during one or more of the clock cycles of a test. Analyze the power dissipation locally, typically in regions determined by the power grid, to avoid excessive local power dissipation even when the total power dissipation is acceptable. Low-power test generation and design-for-testability procedures were developed to address the possibility that scan-based tests will result in excessively high power dissipation. Un-packaged integrated circuits that have potential advantages in circuit density.Power consumption during testing is important since excessive heat dissipation can damage the circuit under test. Since power consumption in test mode is higher than during normal operation, special care must be taken to ensure that the power rating of the SOC is not exceeded during test application.The conflicting goals of low-power scan testing and reduced test data volume appear to be irreconcilable. Test generation for low-power scan testing usually leads to an increase in the number of test vectors. On the other hand, static compaction of scan vectors causes significant increase in power consumption during testing.

Depending on the device being tested, the equipment testing it, and the purpose of test, various types of testing are performed. Below, some commonly used terminologies are discussed.
External Testing. A device is tested by an external device that can be a chip, a board, or a computer or test equipment.
Internal Testing. The tester for a device is in the same packaging as the device. Often, in case of BIST, the tester hardware is integrated with, and on the same chip as the device.
Online Testing. Testing is done while a device is performing its normal functions.
Offline Testing. Device being tested must cease its normal operation, and then be tested. Offline testing can be done by internal or external test hardware.
Concurrent Testing (*Online*). In online testing, concurrent testing is when the normal data the device is using in performing its normal functions are used for testing it.
Concurrent Testing (*ATE*). In ATE terminology, concurrent testing is when a tester is testing various parts of a chip concurrently. For example, the analog, memory, and the logic parts tested at the same time, while the device is on the tester head.

At-Speed Testing. Device being tested at its normal speed of operation. This is also called *AC Testing*.
DC Testing. Device is tested at much slower speed than its operation frequency. This allows all the events to propagate before the outputs are sampled.
In-Circuit Testing. Device being tested is not removed from its mounting place for testing.
Guided Probe Testing. In a process of probing backwards from outputs towards inputs, testing is done to find the source of an error that has appeared on the circuit's outputs.
Diagnostic. Diagnostic is when testing is done to find the cause of failure. There are many other terminologies used for various types of testing that can be told by the context they are used in. As the above terminologies are not standard, they may be used in the literature for slightly different meanings than what we have presented.

II. RELATED WORKS

I. Pomeranz[1] discussed the functional broadside test is conducted by using signal transition pattern. The signal transition pattern is important because to minimize the deviations from functional power dissipation due to arbitrary broadside tests and to search the best pattern matching. Functional broadside tests create functional operation conditions during their two functional capture cycles. First, functional capture cycle is slow functional capture cycle it allows signal transitions at earlier stage. Second, fast functional capture cycle do not exceed possible conditions of functional operation. Pattern test considers second fast functional broadside clock cycle. It guides the generation of low power test sets. Thedeviations donot exceed 0.15 of the number of devices in the circuit.

This is significantly smaller than the activity targeted in switching.These patterns are used to guide the generation of a low-power test set that consists of arbitrary (functional and nonfunctional) broadside tests for transition faults. The test set detects all the detectable transition faults while matching the patterns of signal transitions that are possible during functional operation as well as possible. Pseudo functional scan-based tests are discussed in it to create functional operation conditions during their functional capture cycles. The reachable state must satisfy the pseudo functional scan-based tests based on the computation of functional constraints. Using logic simulation signal patterns of tests are computed.

I. Pomeranz[2] detailed the low power test generation, switching activity is maximized by using functional broadside tests. Functional operation is done on line-by-line basis. The procedures are functional broadside tests, functional broadside templates, computing functional broadside templates, low power test generation procedure. The low power test generation procedure uses functional broadside templates. Delay faults are activated and propagated during second functional clock cycle. The test ends with scan out operation. Fault coverage discussions are not used in it. When the incorporated of generation of functional broadside test and low-power test generation, the fault coverage is used. To introduce the flexibility, limited deviations are allowed from the signal transitions of functional broadside tests. Undetectable faults can be detected by using non-functional broadside tests.

It is assumed that functional operation consists of the application of primary input sequences in functional mode starting from the initial state.Every template uses two type of process they are every fault i.e. f € F and fills the unspecified values of a template based on every test in an arbitrary broadside test sets. The detectable transition faults must be allowed to deviate from signal transitions on line-by-line basis. Computing functional broadside templates starts from completely specified functional broadside tests. The normalized run time is a stronger function of the fault efficiency achieved by functional broadside tests than of the circuit size.

V. Dabholkar, S. Chakravarty, I. Pomeranz, and S. M. Reddy[3] detailed the techniques of BIST (built-in-self-test) technique is used for testing of combinational circuits and reduction of power dissipation. Along with BIST heuristics are used. Two classes of circuits are used namely full integrated scan circuits and combinational circuits. In full integrated scan circuit testing two methods are used test vector ordering and scan latch ordering. Percentage improvement varies between 40% and 60%.In general, the percentage improvement in power dissipation when repetition is allowed is more than the case when no vector is repeated. Percentage improvement varies between 40 and 60%.Power dissipation improvement is achieved by using scan latch ordering with test vector ordering. The scan latch ordering technique has to be applied during the synthesis process, while test-vector ordering can be applied any time before test application. Full scan model achieves power dissipation at every clock cycle.

L. Whetsel[4] ,In integrated circuits, scan architecture is used to test the digital circuitry. The low power scan architecture maintains the test time of conventional architectures. The low power scan architecture reduces test power consumption; it is possible to simultaneously test more die on a wafer than previously possible using conventional scan architectures. This allows wafer test times to be reduced which reduce the manufacturing cost of each die on the wafer. Adapting a known scan path into a scan path of the present invention involves reorganizing the known scan path from being a single scan path containing all the scan cells, into a scan path having a desired number of selectable separate scan paths.

Low power scan path comprising two separate scan paths may reduce power consumption by up to 50%.During operation, each of the two separate scan paths separately charge and discharge one half potentially, of the logic circuitry capacitance charged and discharged by the convention scan path. Further, configuring the same conventional scan path into a low power scan path comprising three separate scan paths may reduce power consumption by up to 66%. During operation, each of the three separate scan paths separately charge and discharge one third potentially, of the logic circuitry capacitance charged and discharged by the convention scan path.

N. A. Touba[5] discussed the test data compression technique, it provides additional on-chip hardware of scan chains in before and after.compression permits the data storage in a compressed form of the tester. It applies data into both pseudorandom and deterministic data. The benefits of test data compression are, it reduces the amount of data storage

which leads to the life extension of testers with limited memory and reduces the test time of given data even for plenty of memory testers. In test compression method test vectors are compressed lossless to preserve fault coverage.

Anshuman Chandraand Krishnendu Chakrabarty[6] proposed a low power scan testing with test data compression. System-on-chip testing concerns two major problem namely test data volume and power consumption. Benchmarks reduced the test data volume and low power scan testing can achieved.the conflicting goals of low-power scan testing and reduced test data volume appear to be irreconcilable. The larger ISCAS 89 benchmarks and for an IBMproduction circuit show that reduced test data volume and low-power scan testing can indeed be achieved.

Kenneth M. Butler,JayashreeSaxena,Tony Fryars ,Graham Hetherington, Atul Jain, Jack Lewis[7] discussedICs have been observed to fail at specified minimum operating voltages during structured at-speed testingwhile passing all other forms of test. Methods exist to reduce power without dramatically increasing pattern volume for a given coverage. Excessive switching power consumption during test can be tackled in multiple ways. Test patterns can be generated to reduce switching activity while possibly increasing pattern volume.

Chakrabathy[8] proposed a selective entries and fixed length indices, a small number of ATE data channels are used to deliver compress data sets. Huffman with variable length coding are used to achieve the normal power consumption. Itdelivers compressed patterns from the tester to the chip and drives a large number of internal scan chains using only a single ATE channel. Hence, the dictionary-based compression technique is especially suitable for reduced-pin count testing, multi-site testing, as well as a low-cost DFT test environment.Test data compression based on selective Huffman coding, the proposed method achieves higher compression for the same amount of hardware overhead, except for the special case when the constraint on the hardware overhead is very small.

III. RESULTS AND DISCUSSIONS

Signal transition pattern are for generation of low power test results substantially different test sets are obtained. Heuristics model based method are used for combinational circuits to minimize the power. Specified templates are used for testing.

IV. CONCLUSION

Here we concluded the discussions about the various testing methodologies and test data compression methods. Scan based architectures also detailed. Low power testing is an major concern,in order to reduce the power.

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